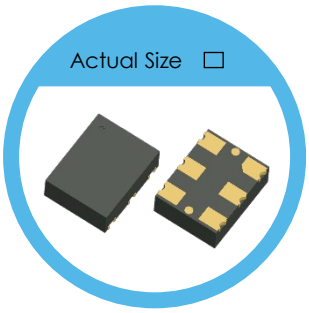
ON-K Type High Frequency & Ultra Low Noise
2.5 x 2.0 mm Differential Output Crystal Oscillator



RoHS Compliant

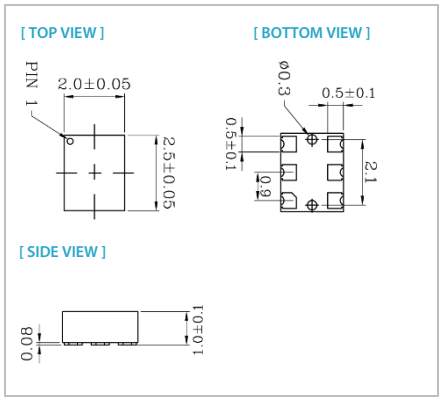
FEATURES

- MSL : Level 1
- Pb-free/RoHS Compliant
- Tri-state Enable / Disable Mode
- Temperature Range: -40 to 85 ˚C
- Clock Output: LVPECL, LVDS, CML, HCSL
- Output Frequency Support from 15MHz to 2.1GHz
- Low Power Supply Voltage: 3.3, 2.5, and 1.8V Supply Options
- Ultra Low Phase RMS jitter: Typical: 150fs at 12kHz to 20MHz Frequency Offsets

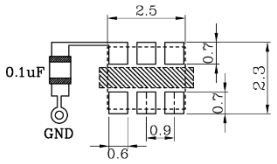
TYPICAL APPLICATION

- SD/HD Video
- Gigabit Ethernet, SONET/SDH
- Storage Area Networking (SAN)
- FPGA Clock Generation

DIMENSION (mm)



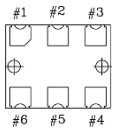
SOLDER PAD LAYOUT (mm)



Please keep the middle area blank. Do not layout any lines in this space.To ensure optimal oscillator performance, place a by-pass capacitor of 0.1µF as close to the part as possible between V_{DD} and GND pads

PIN FUNCTION (mm)

PIN#	FUNCTION
1	NC
2	OE
3	GND
4	Q
5	Qn
6	V_{DD}



ELECTRICAL SPECIFICATION

Parameter		LVPECL 3.3V Min.	LVPECL 3.3V Max.	LVPECL 2.5V Min.	LVPECL 2.5V Max.	Unit	Test Condition
Supply Voltage Variation (V_{DD}) ±10%		2.97	3.63	2.25	2.75	V	
Frequency Range		15	2100	15	2100	MHz	
Standard Frequency		155.52, 156.25, 187.5, 212.5, 266.667, 312.5, 622.08, 644.53125				MHz	
Supply Current			110		95	mA	
Output Level	Output High	V_{DD} – 1.165	V_{DD} – 0.8	V_{DD} – 1.165	V_{DD} – 0.8	V	
	Output Low	V_{DD} – 2.0	V_{DD} – 1.55	V_{DD} – 2.0	V_{DD} – 1.55	V	
Transition Time (20% – 80%)	Rise Time		0.35		0.35	nSec	
	Fall Time		0.35		0.35	nSec	
Duty Cycle		45	55	45	55	%	
Startup Time			8		8	mSec	
Tri-State Mode (Input to Pin 2)	Enable	0.7 x V_{DD}		0.7 x V_{DD}		V	
	Disable		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			110		95	mA	
Phase Noise		Typ.	Max.	Typ.	Max.		
At V_{DD}=3.3V, fout=873.515MHz	1kHz offset	-106		-106		dBc/Hz	
	10kHz offset	-115		-115		dBc/Hz	
	100kHz offset	-123		-123		dBc/Hz	
	1MHz offset	-133		-133		dBc/Hz	
	20MHz offset	-150		-150		dBc/Hz	
RMS Phase Jitter (Integrated 12 kHz~20 MHz)		150	250	150	250	fs	
Period Jitter			50		50	ps	

Note: not all combination of options are available. Other specifications may be available upon request.

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Parameter		LVDS						Unit	Test Condition
		3.3V		2.5V		1.8V			
		Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V_{DD})		2.97	3.63	2.25	2.75	1.71	1.89	V	
Frequency Range		15	2100	15	2100	15	2100	MHz	
Standard Frequency		155.52, 156.25, 187.5, 212.5, 266.667, 312.5, 622.08, 644.53125						MHz	
Supply Current			90		80		70	mA	
Output Level	Output High		1.6		1.6		1.6	V	
	Output Low	0.9		0.9		0.9		V	
Transition Time (20% – 80%)	Rise Time		0.35		0.35		0.35	nSec	
	Fall Time		0.35		0.35		0.35	nSec	
Duty Cycle		45	55	45	55	45	55	%	
Startup Time			8		8		8	mSec	
Tri-State Mode	Enable	0.7 x V_{DD}		0.7 x V_{DD}		0.7 x V_{DD}		V	
(Input to Pin 2)	Disable		0.3 x V_{DD}		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			90		80		70	mA	
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.		
At V_{DD}=3.3V, fout=873.515MHz	1kHz offset	-106		-106		-106		dBc/Hz	
	10kHz offset	-115		-115		-115		dBc/Hz	
	100kHz offset	-123		-123		-123		dBc/Hz	
	1MHz offset	-133		-133		-133		dBc/Hz	
	20MHz offset	-150		-150		-150		dBc/Hz	
RMS Phase Jitter (Integrated 12 kHz~20 MHz)		150	250	150	250	150	250	fs	
Period Jitter			50		50		50	ps	

Parameter		HCSL						Unit	Test Condition
		3.3V		2.5V		1.8V			
		Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V_{DD})		2.97	3.63	2.25	2.75	1.71	1.89	V	
Frequency Range		15	700	15	700	15	700	MHz	
Standard Frequency		155.52, 156.25, 187.5, 212.5, 266.667, 312.5, 622.08, 644.53125						MHz	
Supply Current			90		80		70	mA	
Output Level	Output High	0.66	1.15	0.66	1.15	0.66	1.15	V	
	Output Low	0	0.15	0	0.15	0	0.15	V	
Transition Time (20% – 80%)	Rise Time		0.35		0.35		0.35	nSec	
	Fall Time		0.35		0.35		0.35	nSec	
Duty Cycle		45	55	45	55	45	55	%	
Startup Time			8		8		8	mSec	
Tri-State Mode	Enable	0.7 x V_{DD}		0.7 x V_{DD}		0.7 x V_{DD}		V	
(Input to Pin 2)	Disable		0.3 x V_{DD}		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			90		80		70	mA	
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.		
At V_{DD}=3.3V, fout=805.664MHz	1kHz offset	-107		-107		-107		dBc/Hz	
	10kHz offset	-117		-117		-117		dBc/Hz	
	100kHz offset	-125		-125		-125		dBc/Hz	
	1MHz offset	-135		-135		-135		dBc/Hz	
	20MHz offset	-150		-150		-150		dBc/Hz	
RMS Phase Jitter (Integrated 12 kHz~20 MHz)		150	250	150	250	150	250	fs	
Period Jitter			50		50		50	ps	

Parameter		CML						Unit	Test Condition
		3.3V		2.5V		1.8V			
		Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V_{DD})		2.97	3.63	2.25	2.75	1.71	1.89	V	
Frequency Range		15	2100	15	2100	15	2100	MHz	
Standard Frequency		155.52, 156.25, 187.5, 212.5, 266.667, 312.5, 622.08, 644.53125						MHz	
Supply Current			90		80		70	mA	
Output Level	Output High	V_{DD} – 0.085	V_{DD}	V_{DD} – 0.085	V_{DD}	V_{DD} – 0.085	V_{DD}	V	
	Output Low	V_{DD} – 0.6	V_{DD} – 0.32	V_{DD} – 0.6	V_{DD} – 0.32	V_{DD} – 0.6	V_{DD} – 0.32	V	
Transition Time (20% – 80%)	Rise Time		0.35		0.35		0.35	nSec	
	Fall Time		0.35		0.35		0.35	nSec	
Duty Cycle		45	55	45	55	45	55	%	
Startup Time			8		8		8	mSec	
Tri-State Mode	Enable	0.7 x V_{DD}		0.7 x V_{DD}		0.7 x V_{DD}		V	
(Input to Pin 2)	Disable		0.3 x V_{DD}		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			90		80		70	mA	
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.		
At V_{DD}=3.3V, fout=805.664MHz	1kHz offset	-107		-107		-107		dBc/Hz	
	10kHz offset	-117		-117		-117		dBc/Hz	
	100kHz offset	-125		-125		-125		dBc/Hz	
	1MHz offset	-135		-135		-135		dBc/Hz	
	20MHz offset	-150		-150		-150		dBc/Hz	
RMS Phase Jitter (Integrated 12 kHz~20 MHz)		150	250	150	250	150	250	fs	
Period Jitter			50		50		50	ps	

Note: not all combination of options are available. Other specifications may be available upon request.

Specifications subject to change without notice.

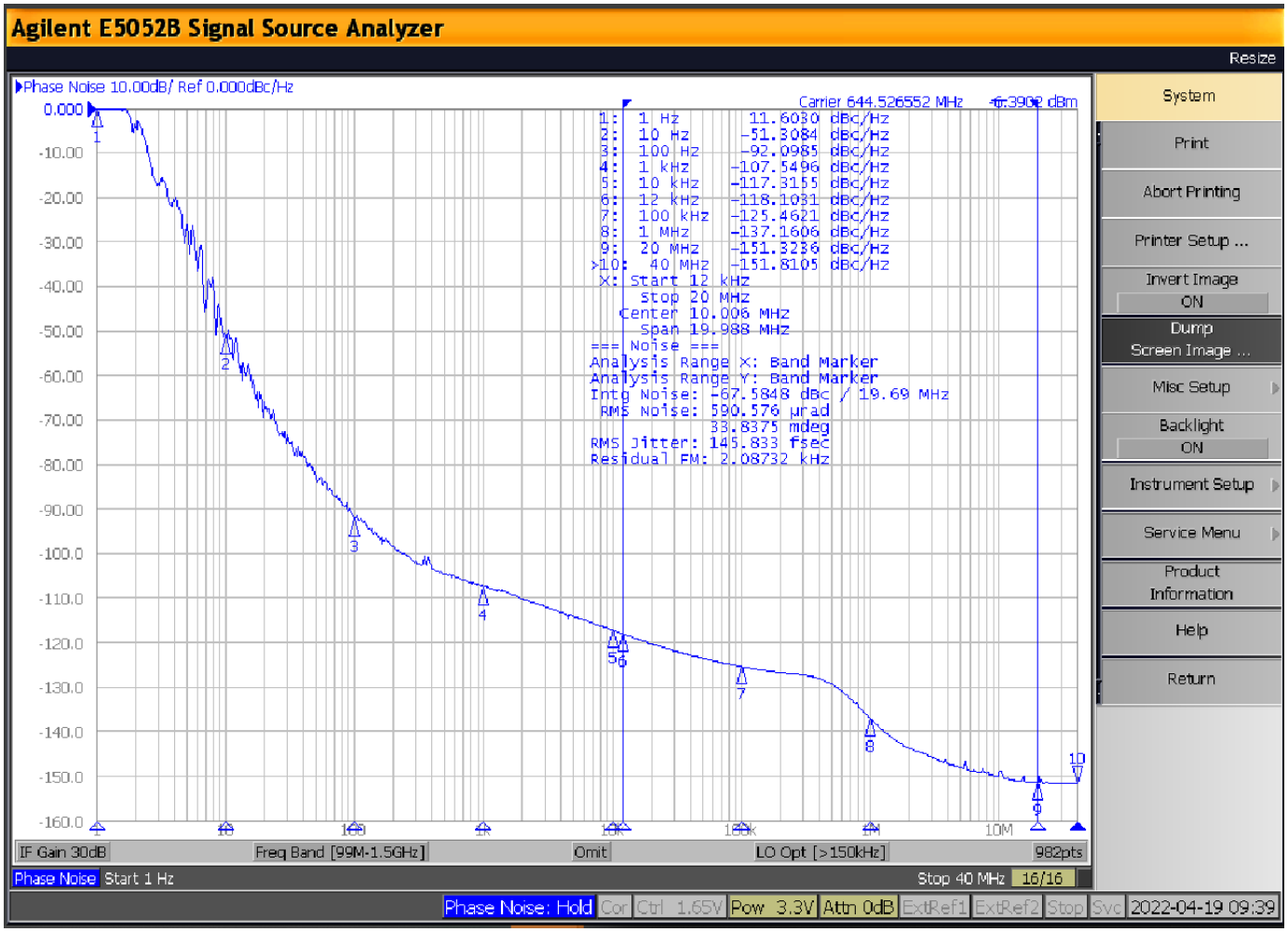
FREQ. STABILITY vs. TEMP. RANGE

ppm / Temp.(°C)	±20	±25	±50	±100
-10 ~ +60	○	○	○	○
-20 ~ +70	△	○	○	○
-40 ~ +85	×	△	○	○

○: Available △:Conditional ×: Not Available
Inclusive of calibration @ 25°C ,operating temperature rrange,input Voltage variation,load variation,aging (1st year),shock,and vibration

Phase Noise Test Data

Output level: LVPECL, Fout=644.53125MHz, V_{DD}=3.3V → Phase RMS Jitter: 145.8fsec



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